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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. END920010115US2

In Re Application Of: **Darbha et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/629,469	7/29/2003	Nguyen, Dilinh P.	30449	2814	

Invention: **STRESS REDUCTION IN FLIP-CHIP PBGA PACKAGING BY UTILIZING SEGMENTED CHIPS AND/OR CHIP CARRIERS**

COMMISSIONER FOR PATENTS:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Darbha *et al.*

Art Unit: 2814

Serial No.: 10/629,469

Dkt. No.: END920010115US2

Filed: 7/29/2003

Examiner: Nguyen, Dilinh P.

Title: **STRESS REDUCTION IN FLIP-CHIP PBGA PACKAGING BY UTILIZING SEGMENTED CHIPS AND/OR CHIP CARRIERS**

Commissioner for Patents
P.O. Box 1450
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BRIEF OF APPELLANTS

This Appeal Brief, pursuant to the Notice of Appeal filed November 19, 2004, is an appeal from the rejection of the Examiner dated June 28, 2004.

REAL PARTY IN INTEREST

IBM Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAMS

Claims 9-11, 13, 21, 23, 25, 26, 28, and 30-32 remain pending. This Brief is in support of an appeal from the final rejection.

STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

SUMMARY OF INVENTION

The present invention discloses a electronic structure and method for forming the electronic structure. The electrical structure comprises a substrate and a semiconductor device divided into a plurality of segments electrically coupled to the substrate. See Specification, page 6, lines 10-14. The method for forming the electronic structure comprises dividing the semiconductor device into a plurality of segments and electrically coupling a substrate to each segment of the plurality of segments of the semiconductor device to the substrate. See Specification, page 6, line 21- page 7, line 2. The substrate may selected from the group consisting of a ceramic chip carrier, an organic chip carrier, and a printed circuit board. See Specification, page 6, lines18-19. At least one segment of the plurality of segments of the semiconductor device is not congruent with respect to a remaining segment of the plurality segments of the semiconductor device. See Specification, page 7, lines10-11. The substrate comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device. See Specification, page 6, lines19-21. A length of each segment of the plurality of segments of the semiconductor device may be greater than or equal to

5 millimeters. See Specification, page 6, lines15-16. A first segment and a second segment of the plurality of segments may be congruent with respect to each other. See Specification, page 7, lines 9-11. Each of the plurality of segments may be square segments. See Specification, page 7, lines12-15. The substrate may be symmetrically coupled to each segment of the plurality of segments. See Specification, page 5, lines17-18. The semiconductor device may be a semiconductor chip. See Specification, page 6, line 12.

ISSUES

1. Whether claims 9, 11, 13, 21, 23, 25-26, 28 and 31-32 are unpatentable under U.S.C. §103(a) over Fillion (U.S. Patent Number 5,353,498) in view of Nagarajan (U.S. Patent Number 6,639,321).

2. Whether claims 10 and 30 are unpatentable under U.S.C. §103(a) over Fillion (U.S. Patent Number 5,353,498) in view of Nagarajan (U.S. Patent Number 6,639,321) and in further view of Saito (U.S. Patent Number 5,479,335).

GROUPING OF CLAIMS

Group	Issue	Claims	Do Claims of Group Stand or Fall Together?
1	1	9, 11, 13, 21, and 23	Yes
2	1	25, 26, 28, 31 and 32	Yes
3	2	10 and 30	Yes

Groups 1 and 2 include the claims corresponding to Issue 1. Group 3 includes the claims corresponding to Issue 2. Claims 9, 11, 13, 21, and 23 of group 1 stand or fall together. Claims 25, 26, 28, 31 and 32 of group 2 stand or fall together. Claims 10 and 30 of group 3 stand or fall together. The claims of Group 1 (associated with Issue 1) do not stand or fall together with the claims of Group 2 (associated with Issue 1), because the claims of group 1 are structure claims and the claims of group 2 are method claims and therefore the claims of group 1 comprise a different statutory class than the claims of group 2. The claims of Group 1 or Group 2 do not stand or fall together with the claims of Group 3 (associated with Issue 2), because the claims of Groups 1 and 2 and the claims of Group 3 are rejected over different combinations of references.

ARGUMENT

Issue 1, Group 1

CLAIMS 9, 11, 13, 21, 23, 25-26, 28 and 31-32 ARE NOT UNPATENTABLE UNDER U.S.C. §103(a) OVER FILLION (US 5,353,498) IN VIEW OF NAGARAJAN (US 6,639,321).

The Examiner rejected claims 9, 11, 13, 21, 23, 25-26, 28 and 31-32 under U.S.C. §103(a) over Fillion (U.S. Patent Number 5,353,498) in view of Nagarajan (U.S. Patent Number 6,639,321).

The Examiner alleges that " Regarding claims 9 and 25, Fillion et al. disclose a semiconductor device comprising:

a substrate 10, wherein the substrate is selected from the group consisting of a ceramic chip carrier, an organic chip carrier (fig. 1a, column 5, lines 16-18);

a semiconductor device 14 electrically coupled to the substrate, wherein the semiconductor device is divided into a plurality of segments, wherein at least one segment of the plurality of segments is not congruent with respect to a remaining segment of the plurality of segments.

Fillion et al. fail to disclose the substrate comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device. Nagarajan et al. disclose a semiconductor device (cover fig.) comprising: a substrate 108 comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device 202 (column 5, lines 1923). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify

the device of Fillion et al. to reduce mismatch of a coefficient of thermal expansion of the die with the substrate, as shown by Nagarajan et al.

Regarding claims 11 and 28, Fillion et al. disclose a first segment and a second segment of the plurality of segments 14 are congruent with respect to each other (fig. 1 a).
Regarding claims 13 and 31, Fillion et al. disclose the plurality of segments are square segments (fig. 4d).

Regarding claim 21, Fillion et al. disclose the substrate is symmetrically coupled to each segment of the semiconductor device (fig. 1 a).

Regarding claims 23 and 32, Fillion et al. disclose the semiconductor device is a semiconductor chip (fig. la, column 5, lines 23).

Regarding claim 26, Fillion et al. disclose each segment of the semiconductor device is symmetrically coupled to the substrate (fig. 1a) ".

Claim 9

Appellants respectfully contend that the rejection of claim 9 under 35 U.S.C. §103(a) as allegedly being unpatentable over Fillion et al. in view of Nagarajan et al. is improper because Appellants respectfully contend that the Examiner has not provided a persuasive reason for modifying Fillion by the alleged teaching of Nagarajan for rejecting claim 9. The only basis that the Examiner provides for modifying Fillion with Nagarajan is that Nagarajan teaches a substrate 108 comprising a coefficient of thermal expansion greater that a coefficient of thermal expansion of a semiconductor device 202. The Examiner alleges that " it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fillion

et al. to reduce mismatch of a coefficient of thermal expansion of the die with the substrate, as shown by Nagarajan et al ". In response, Appellants contend that the Examiner has incorrectly concluded that modifying the device of Fillion with the "substrate 108 comprising a coefficient of thermal expansion greater that a coefficient of thermal expansion of a semiconductor device 202 " of Nagarajan will reduce "a mismatch of a coefficient of thermal expansion between the die and the substrate ". Appellants contend that Nagarajan does **not teach reducing a mismatch of a coefficient of thermal expansion** by using a substrate with a greater coefficient of thermal expansion than that of a semiconductor device as alleged by the Examiner. In contrast, Nagarajan teaches in col. 2, lines 3-5, "**a die thickness reduced** from a wafer thickness **to reduce mismatch of a coefficient of thermal expansion** between the thin die and a substrate". Nagarajan further teaches in col. 3, line 67- col. 4, line 5, " The **combination** of **the thin die** 202 **with the thin film layers** 230, 232, and 234 has a composite coefficient of thermal expansion of about 15-19 parts per million per degree Kelvin that **reduces mismatch of coefficient of thermal expansion** of the thin die 202 with the laminated substrate 108 ". Therefore Appellants contend that Nagarajan teaches a reduction of a coefficient of thermal expansion by reducing a die thickness and adding thin film layers and **not** by using a substrate with a greater coefficient of thermal expansion than that of a semiconductor device as alleged by the Examiner.

In summary, Appellants maintain that the Examiner has not persuasively demonstrated that it is obvious to modify Fillion with Nagarajan for the purpose of rejecting claim 9. Accordingly, Appellants contend that the Examiner has not disclosed a teaching or suggestion in the prior art that supports the modification. Therefore, Applicants contend that Fillion and Nagarajan may not be combined for the purpose of rejecting claim 9. Accordingly, Appellants

contends that the Examiner has not established a *prima facie* case of obviousness in relationship to claim 9. Based on the preceding argument, Appellants maintain that claim 9 is not unpatentable over Fillion in view of Nagarajan.

Claim 11

Since claim 11 depends from claim 9, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 11 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 13

Since claim 13 depends from claim 9, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 13 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 21

Since claim 21 depends from claim 9, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 21 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 23

Since claim 23 depends from claim 9, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 23 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Issue 1, Group 2

Claim 25

Appellants present two arguments as to why claim 25 is not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 25: First Argument

A first argument as to why claim 25 is not unpatentable over Fillion in view of Nagarajan, is that Appellants respectfully contend that Fillion and Nagarajan do not individually or collectively teach or suggest each and every feature of claim 25. For example, Fillion and Nagarajan do not teach or suggest the feature of "**dividing** a semiconductor device into a plurality of segments " (emphasis added). Fillion and Nagarajan do not teach or suggest that a semiconductor device is **divided** into a plurality of segments as taught by Appellant's claim 25. In contrast, Fillion teaches a plurality of chips14 **placed** on a surface (e.g., base sheet 12, see Nagarajan, col. 5, lines 22-35, FIG. 1a, and claim 1). Nagarajan do not disclose any method of fabricating the plurality of chips 14 for placement on a surface as taught by Appellant's claim 25 and most certainly does not teach the "**dividing**" step of claim 25. Therefore Appellant's

contend that Fillion and Nagarajan do not teach or suggest the preceding features of claim 25 and the Examiner has failed to establish a *prima facie* case of obviousness in relation to claim 29.

Based on the preceding first argument, Appellants maintain that claim 25 is not unpatentable over Fillion in view of Nagarajan.

Claim 25: Second Argument

A second argument as to why claim 25 is not unpatentable over Fillion in view of Nagarajan, is that Appellants respectfully contend that the rejection of claim 25 under 35 U.S.C. §103(a) as allegedly being unpatentable over Fillion et al. in view of Nagarajan et al. is improper because Appellants respectfully contend that the Examiner has not provided a persuasive reason for modifying Fillion by the alleged teaching of Nagarajan for rejecting claim 25. The only basis that the Examiner provides for modifying Fillion with Nagarajan is that Nagarajan teaches a substrate 108 comprising a coefficient of thermal expansion greater that a coefficient of thermal expansion of a semiconductor device 202. The Examiner alleges that " it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fillion et al. to reduce mismatch of a coefficient of thermal expansion of the die with the substrate, as shown by Nagarajan et al ". In response, Appellants contend that the Examiner has incorrectly concluded that modifying the device of Fillion with the "substrate 108 comprising a coefficient of thermal expansion greater that a coefficient of thermal expansion of a semiconductor device 202 " of Nagarajan will reduce "a mismatch of a coefficient of thermal expansion between the die and the substrate ". Appellants contend that Nagarajan does **not teach reducing a mismatch of a coefficient of thermal expansion** by using a substrate with a

greater coefficient of thermal expansion than that of a semiconductor device as alleged by the Examiner. In contrast, Nagarajan teaches in col. 2, lines 3-5, "**a die thickness reduced** from a wafer thickness **to reduce mismatch of a coefficient of thermal expansion** between the thin die and a substrate". Nagarajan further teaches in col. 3, line 67- col. 4, line 5, " The **combination** of **the thin die** 202 **with the thin film layers** 230, 232, and 234 has a composite coefficient of thermal expansion of about 15-19 parts per million per degree Kelvin that **reduces mismatch of coefficient of thermal expansion** of the thin die 202 with the laminated substrate 108 ". Therefore Appellants contend that Nagarajan teaches a reduction of a coefficient of thermal expansion by reducing a die thickness and adding thin film layers and not by using a substrate with a greater coefficient of thermal expansion than that of a semiconductor device as alleged by the Examiner.

In summary, Appellants maintain that the Examiner has not persuasively demonstrated that it is obvious to modify Fillion with Nagarajan for the purpose of rejecting claim 25. Accordingly, Appellants contend that the Examiner has not disclosed a teaching or suggestion in the prior art that supports the modification. Therefore, Applicants contend that Fillion and Nagarajan may not be combined for the purpose of rejecting claim 25. Accordingly, Appellants contends that the Examiner has not established a *prima facie* case of obviousness in relationship to claim 25.

Based on the preceding second argument, Appellants maintain that claim 25 is not unpatentable over Fillion in view of Nagarajan.

Claim 26

Since claim 26 depends from claim 25, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 26 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 28

Since claim 28 depends from claim 25, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 28 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 31

Since claim 31 depends from claim 25, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 31 is likewise not unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a).

Claim 32

Since claim 32 depends from claim 25, which Appellants have argued *supra* to not be unpatentable over Fillion et al. in view of Nagarajan under 35 U.S.C. §103(a), Appellants maintain that claim 32 is likewise not unpatentable over Fillion et al. in view of Nagarajan under

35 U.S.C. §103(a).

Issue 2, Group 3

CLAIMS 10 AND 30 ARE NOT UNPATENTABLE UNDER U.S.C. §103(a) OVER FILLION (U.S. 5,353,498) IN VIEW OF NAGARAJAN (U.S. 6,639,321) AND IN FURTHER VIEW OF SAITO (U.S. 5,479,335).

The Examiner rejected claims 10 and 30 under U.S.C. §103(a) over Fillion (U.S. Patent Number 5,353,498) in view of Nagarajan (U.S. Patent Number 6,639,321) and in further view of Saito (U.S. Patent Number 5,479,335).

The Examiner alleges that " Fillion et al. and Nagarajan et al. fail to disclose the length of each segment of the semiconductor device is greater than or equal to 5 millimeters ".

The Examiner alleges that "Saito et al. disclose a device comprising: a chip size is from a few millimeters square to 20 millimeters square (column 14, lines 9-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fillion et al. and Nagarajan et al. to reduce the chip size and improve the device's efficiency, as shown by Saito et al ".

Appellants contend that the rejection of claims 10 and 30 over Fillion in view of Nagarajan and in further view of Saito under 35 U.S.C. §103(a) is improper because the Examiner has not established that Fillion, Nagarajan, and Saito individually or collectively teach or suggest each and every feature of claims 10 and 30. For example, Fillion, Nagarajan, and Saito do not teach or suggest the feature of "the length of each segment of the semiconductor device is greater than or equal to **5 millimeters** " (emphasis added). Fillion, Nagarajan, and Saito do not teach or suggest segments of a semiconductor device that each comprise a **length** of at least **5 millimeters**. Appellants contend that the Examiner has incorrectly concluded that Saito

teaches all of the features of claims 10 and 30. The Examiner alleges that " Saito et al. disclose a device comprising: a chip size is from a few millimeters square to **20 millimeters square** (column 14, lines 9-10) ". Therefore, Saito teaches a chip size that is not greater than 20 millimeters square. Appellants contend that **20 millimeters square** is an **area** corresponding to a **length equaling a square root of 20 or about 4.47 millimeters** which is **less** than a length of at least **5 millimeters** as taught by Appellants claims 10 and 30. Therefore, Appellants contend that Saito does not teach a length of a segment of a semiconductor device greater than or equal to **5 millimeters**. Accordingly, Appellants maintain that the Examiner has not provided any support to demonstrate that Fillion, Nagarajan, and Saito teach or suggest the aforementioned feature of claims 10 and 30 and therefore appellants contend that the Examiner has not established a *prima facie* case of obviousness in relationship to claims 10 and 30.

For the preceding reason, Applicant maintains that claims 10 and 30 are not obvious and thus cannot be rejected over Fillion and Nagarajan together with Saito under 35 U.S.C. §103(a). Accordingly, Applicants maintain that claims 10 and 30 are in condition for allowance.

In summary, Appellants respectfully request reversal of the June 28, 2004 Office Action rejection of claims 9-11, 13, 21, 23, 25, 26, 28, and 30-32.

Respectfully submitted,

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APPENDIX - CLAIMS ON APPEAL

9. An electronic structure, comprising:

a substrate, wherein the substrate is selected from the group consisting of a ceramic chip carrier, an organic chip carrier, and a printed circuit board; and

a semiconductor device electrically coupled to the substrate, wherein the semiconductor device is divided into a plurality of segments, wherein at least one segment of the plurality of segments is not congruent with respect to a remaining segment of the plurality segments, and wherein the substrate comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device.

10. The electronic structure of claim 9, wherein the length of each segment of the semiconductor device is greater than or equal to 5 millimeters.

11. The electronic structure of claim 9, wherein a first segment and a second segment of the plurality of segments are congruent with respect to each other.

13. The electronic structure of claim 9, wherein the plurality of segments are square segments.

21. The electronic structure of claim 9, wherein the substrate is symmetrically coupled to each segment of the semiconductor device.

23. The electronic structure of claim 9, wherein the semiconductor device is a semiconductor chip.

25. A method for forming an electronic structure, comprising:

dividing a semiconductor device into a plurality of segments, and

electrically coupling a substrate to each segment of the plurality of segments of the semiconductor device, wherein the substrate is selected from the group consisting of a ceramic chip carrier, an organic chip carrier, and a printed circuit board, wherein at least one segment of the plurality of segments is not congruent with respect to a remaining segment of the plurality of segments, and wherein the substrate comprises a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of the semiconductor device.

26. The method of claim 25, wherein each segment of the semiconductor device is symmetrically coupled to the substrate.

28. The method of claim 25, wherein a first segment and a second segment of the plurality of segments are congruent with respect to each other.

30. The method of claim 25, wherein the length of each segment of the semiconductor device is greater than or equal to 5 millimeters.

31. The method of claim 25, wherein the plurality of segments are square segments.

32. The method of claim 25, wherein the semiconductor device is a semiconductor chip.